

Pantelis Patsaoglou

Ioannina, Greece | [linkedin.com/in/patsaoglou-pantelis/](https://www.linkedin.com/in/patsaoglou-pantelis/)

EDUCATION

University of Ioannina | *Department of Computer Science & Computer Engineering* **10/2020 – 07/2025**

- ***Integrated Master's Diploma with specialty in Electronics Engineering***
- **Diploma Grade:** 7.33/10
- **Thesis Subject:**
 - *Study and Design of basic stages in Phase-Locked Loop (PLL)*
 - LC-VCO, Charge Pumps, Rail-to-Rail Operational Amplifiers, Frequency Dividers, Digital Design, Analog Design, Cadence Suite, Phase Noise Analysis, PVT Variations
- **Interests:**
 - Analog/Digital Design (Integrated Circuits, Hardware Design)
 - Hardware Applications (Embedded Hardware, IoT)
 - Computer Systems (Embedded Systems, Operating Systems)

Languages:

- **Greek** (*Bilingual*)
- **English** (*B2 Level FCE*)

SKILLS

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|-----------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| • IC/Hardware Design tools: | Cadence Virtuoso/Spectre, Altium Designer, Kicad, LT-Spice, VHDL, Verilog, Verilog-A, Quartus/ModelSim |
| • Hardware design: | Analog/Digital and Mixed Signal hardware applications (Multilayer PCBs, MCU/MPU, DDR, Low Power/Energy Harvesting designs) |
| • Firmware development: | Proficiency in C/C++ firmware programming (STM32 HAL, ESP-32 IDF, RTOS), experience with kernel module development, peripheral driver development, familiarity with RISC-V Architecture/Assembly |
| • Requirements Analysis: | Meeting design specifications, component selection, reading hardware documentation (Datasheets/Schematics) |
| • In lab experience: | Oscilloscopes, Power Supplies, SMT microsoldering, hardware prototyping and debugging |
| • Design limitations/issues awareness: | Manufacturing issues in Circuit/PCB development and layout challenges (EMC, Power/Signal Integrity) |

- **IoT Stacks/Architectures:** LoraWAN, MQTT, ChirpStack
- **Project Version Control tools:** Git, GitHub, GitLab
- **Software Development:** Octave, Python, Java, MySQL (Spring Boot, FastAPI)

EXPERIENCE

IQSoft | Hardware Design/Firmware Development *Ioannina, Greece* | **07/2023 – 09/2023** (*Full-time*)
| **10/2023 – 01/2024** (*Part-time*)

- I was assigned the re-design of the Terraweb Control Box Motherboard (*TCB V7*):
 - Requirements meetup (USB Communication with the TCB PC, external power control, remote control via a GSM module, SD file system setup for sensor, voltage, TCB events logging and user option profiles)
 - PCB Layout Stages (went through different hardware solutions/versions to meet requirements and reliable functionality)
 - Firmware Development (main functionality, peripheral drivers and USB Serial Communication API, working along with the software team to create a Web application that uses the API and offers a visual interface for TCB configuration to the End User)

ACADEMIC ACTIVITIES

- **Lab Assistance:**
 - Basic Electronics Course Lab (2023-2024-2025)
 - Analog Electronics Design (2024)

PROFESSIONAL ACTIVITIES

- **The Things Conference** | IoT Event *Amsterdam, The Netherlands* | **2023 – 2025**
- **Bosch Spring School Event** *Reutlingen, Germany* | **06/03 – 07/03/2024**
AI applications on Semiconductor Manufacturing (selected among 50 individuals)
- **PAnhellenic Conference on Electronics and Telecommunications** *Thessaloniki, Greece* | **2024**
- **Open Source Summit** | Linux Foundation *Vienna, Austria* | **16/10 – 18/10/2024**
- **TechFuse Hackathon 2025** | IoT Environmental Monitoring Solution *Ioannina, Greece* | **15/03/2025**

EXTERNAL LINKS

- **Website:** dreamxlabsgroup.github.io/ (Portfolio)
- **GitHub:** github.com/patsaoglou
- **Linkedin:** [linkedin.com/in/patsaoglou-pantelis/](https://www.linkedin.com/in/patsaoglou-pantelis/)

REFERENCES

- **Available – Upon Request**